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Total Number of Pages in This Submission: 28

Application Number	10/661,037
Filing Date	09/12/2003
First Named Inventor	John D. Hyde
Art Unit	2822
Examiner Name	Soward, Ida M.
Attorney Docket Number	IMPJ-0003D1 (033327-056)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
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  - ☐ Affidavits/declaration(s)
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- ☐ Information Disclosure Statement
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- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:

Postcard, Resp. to Notification of Non-Compliant Appeal Brief (1 pg.), Revised Appeal Brief (26 pgs.)

Remarks

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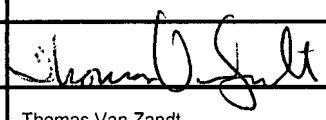
Signature			
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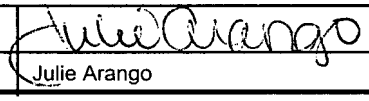
Signature			
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	John D. Hyde et al.	CONFIRMATION NO.:	6704
SERIAL NO.:	10/661,037		
FILING DATE:	09/12/2003		
TITLE:	$_{P}$FET SYNAPSE TRANSISTOR WITH STRUCTURE FOR FACILITATING CHARGE INJECTION AND/OR TUNNELING WITH RESPECT TO A FLOATING GATE		
EXAMINER:	Soward, Ida M.		
ART UNIT:	2822		

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RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed May 2, 2007, enclosed please find a revised Appeal Brief in compliance with 37 C.F.R. 41.37.

Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-1698.

Respectfully submitted,
THELEN REID BROWN RAYSMAN & STEINER LLP

Dated: 06/04/2007

Thomas Van Zandt
Reg. No. 43,219

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Date: 06/04/2007 Name: Julie Arango
Julie Arango

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REVISED APPEAL BRIEF

Dear Sir:

This paper is in support of a Notice to Appeal filed November 27, 2006, of the Office Action dated August 24, 2006, to the Board of Patent Appeals and Interferences.

Table of Contents

Real Party in Interest

Impinj, Inc.

Related Appeals and Interferences

None.

Status of Claims

Claims 1-35 and 41-43 have been canceled.

Claims 36-40 and 44-52 have been finally rejected and are on appeal.

Status of Amendments

All amendments have been entered. No After Final amendments have been filed.

Summary of Claimed Subject Matter

The invention relates to synapse transistors, as used for example in Digital-to-Analog Converters (DACs). A conceptual circuit model 10 of a synapse transistor 11 is shown in FIG. 1, and a structure view of the device is provided in FIGS. 2A and 2B. The synapse transistor is discussed for example in page 9, line 1 through page 12, line 13. As described therein, synapse transistor 11[1] includes two devices—a first, readout transistor 12, and a second, tunneling junction 14[2]. Both devices are shown, in the example given, to be specifically-configured pFET (p-channel Field Effect Transistor) devices that are formed in a p- substrate 20. For the first, readout transistor 12, described in for example para. [0012], a first n- well 22 is provided in the substrate 20.[3] Formed in the first n- well 22 are a pair of p+ doped regions 26, 28 providing, respectively, a source and a drain for the readout transistor.[4] The source 26 and drain 28 are provided with respective source and drain contact terminals 44 and 46,[5] while the first n- well 22 is provided with a well contact terminal 47[6] coupled to the first n- well 22 by way of a n+ region 49 formed in the n- well. Between the source 26 and drain 28 in n- well 22 is a channel 30,[7] over which is disposed a gate oxide layer 32 that insulates a floating gate 16 formed atop the readout transistor 12.[8]

The second device—tunneling junction 14—is in the form of a second n- well 24 formed in p- substrate 20. A source 36 and a drain 38 are formed in the second n- well 24, and these are shorted together by a conductor 40.[9] The second n- well 24 is provided with a well contact terminal 48[10] coupled to the second n- well 24 by way of a n+ region formed in the n- well. Floating gate 16 extends over tunneling junction 14 as well as over readout transistor 12 and is

[1] P. 9, l. 20 – p. 10, l. 1.
[2] P. 12, ll. 3-6.
[3] P. 10, ll. 18-19.
[4] P. 10, l. 20 – p. 11, l. 1.
[5] P. 11, ll. 21-22.
[6] P. 11, ll. 22-23.
[7] P. 11, ll. 1-2.
[8] P. 11, ll. 2-6.
[9] P. 11, l. 13.
[10] P. 11, l. 22.

thus common to both devices. Floating gate 16 is kept isolated from second n- well 24 by gate oxide region 32.

Floating gate 16, which, as explained above, is shared by both the readout transistor 12 and the tunneling junction 14, provides key functionality to the synapse transistor 11. Specifically, using a controlled application of voltage bias to the various contacts (44, 46, 47, 48) of the synapse transistor 11, charge (electrons) can be injected across the gate oxide layer 32 and onto the floating gate 16 from the channel region 30 using readout transistor 12. Similarly, charge can be tunneled from the floating gate 16 across the gate oxide layer 32 using tunneling junction 14. Adding or removing charge from the floating gate 16 can be effected during initial fabrication, relying on the ability of the floating gate to indefinitely retain the charge so added or removed. Alternatively or in addition, adding or removing charge can be effected continuously "on-the-go" during normal operation. Such control of the amount of charge on the floating gate 16 provides a very precise mechanism for influencing the various operational parameters of the synapse transistor. This influence, in the exemplary context of a digital-to-analog converter, enables very high resolution devices having very compact size.

Claim 36 relates to a pFET synapse transistor as detailed[11] in FIGS. 2A and 2B, and recites a p- doped substrate (20),[12] a first n- well (22)[13] and a second n- well (24)[14] disposed in the p- doped substrate, a first p+ doped region (26) disposed in the first n- well forming a source and a second p+ doped region (28) disposed in the first n- well forming a drain, and a channel (30) disposed in the first n- well between the source and drain. Claim 1 further recites a third p+ doped region (36) and a fourth p+ doped region (38) disposed[15] in the second n- well (24), the third p+ doped region and said fourth p+ doped region together forming a tunneling junction. Claim 1 further recites a layer of gate oxide (32) disposed above the channel (30), the first n- well (22) and the second n- well (24), and a polysilicon floating gate (16) disposed above the layer of gate oxide (32). Claim 1 further recites a source contact terminal (44) electrically

[11] See also P. 9, l. 20 – p. 10, l. 1.
[12] P. 10, ll. 18-19.
[13] P. 10, l. 19.
[14] P. 10, l. 20.
[15] P. 11, l. 12.

coupled to the source (26), a drain contact terminal (46) electrically coupled to the drain (28), and a well contact terminal (48) electrically coupled to the second n- well (24). (The recited source and drain contact terminals may also refer to portions of the conductor 40 shorting together source 36 and drain 38 in second n- well 22).[16]

Claim 38 also relates to a pFET synapse transistor and recites a p- doped substrate (20),[17] a first n- well (22)[18] and a second n- well (24)[19] disposed in the p- doped substrate, a first p+ doped region (26)[20] disposed in the first n- well forming a source and a second p+ doped region (28)[21] disposed in the first n- well forming a drain, and a channel (30)[22] disposed in the first n- well (22) between the source (26) and drain (28). Claim 1 further recites a third p+ doped region (36)[23] and a fourth p+ doped region (38)[24] disposed in the second n- well, the third and fourth p+ doped regions together forming a tunneling junction. Claim 1 further recites a layer of gate oxide (32)[25] disposed above the channel (30), the first n- well (22) and the second n- well (24), and a polysilicon floating gate (16) disposed above the layer of gate oxide (32).[26] Claim 1 further recites a source contact terminal (44)[27] electrically coupled to the source, a drain contact terminal (46)[28] electrically coupled to the drain, and a well contact terminal (48)[29] electrically coupled to the second n- well, wherein the third (36)[30] and fourth (38)[31] p+ doped regions are shorted together with a conductive layer (40)[32] which forms a bridge over the floating gate (16) and wherein the well contact terminal (48) is strapped to the third (36) and fourth (38) p+ doped regions.

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[16] P. 11, ll. 12-13.
[17] P. 10, ll. 18-19.
[18] P. 10, l. 19.
[19] P. 10, l. 20.
[20] P. 10, l. 21.
[21] P. 10, l. 21.
[22] P. 11, ll. 1-2.
[23] P. 11, l. 12.
[24] P. 11, l. 12.
[25] P. 11, l. 2.
[26] P. 11, ll. 2-6.
[27] P. 11, l. 21.
[28] P. 11, l. 22.
[29] P. 11, l. 22
[30] P. 11, l. 22
[31] P. 11, l. 22.
[32] P. 11, l. 13.

Claim 44 relates to a pFET synapse transistor and recites a p- doped substrate (20),[33] a first n- well (22)[34] and a second n- well (24)[35] disposed in the substrate, a first p+ doped region (26)[36] disposed in the first n- well forming a source and a second p+ doped region (28)[37] disposed in the first n- well forming a drain, a channel (30)[38] disposed in the first n- well between the source and drain, and a third p+ doped region (36)[39] and a fourth p+ doped region (38)[40] disposed in the second n- well, the third p+ region and said fourth p+ region together forming a tunneling junction. Claim 44 further recites a layer of gate oxide (32)[41] disposed above the channel, the first n- well and the second n- well, a polysilicon floating gate (16)[42] disposed above the layer of gate oxide, a source contact terminal (44)[43] electrically coupled to the source, a drain contact terminal (46)[44] electrically coupled to the drain, and a well contact terminal (48)[45] electrically coupled to the second n- well. According to Claim 44, the synapse transistor is configured to operate as a current source without gate input using a single polysilicon gate layer.

Claim 45 relates to a system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip. The system comprises a pFET synapse transistor (11) including a p- doped substrate(20), a first n- well (22) and a second n- well (24) disposed in the substrate, a first p+ doped region (26) disposed in the first n- well forming a source and a second p+ doped region (28) disposed in the first n- well forming a drain, a channel (30) disposed in the first n- well between the source and drain, and a third p+ doped region (36) and a fourth p+ doped region (38) disposed in the second n- well, the third p+ region and said fourth p+ region together forming a tunneling junction. Claim 45 further includes a layer of gate oxide (32) disposed above the channel, the first n- well and the second n- well, a polysilicon floating gate

[33] P. 10, ll. 18-19.
[34] P. 10, l. 19.
[35] P. 10, l. 20.
[36] P. 10, l. 21.
[37] P. 10, l. 21.
[38] P. 11, l. 1-2.
[39] P. 11, l. 12.
[40] P. 11, l. 12.
[41] P. 11, l. 2.
[42] P. 9, ll. 5-6.
[43] P. 11, ll. 21-22.
[44] P. 11, ll. 21-22.
[45] P. 11, l. 22.

(16)[46] disposed above the layer of gate oxide, a source contact terminal (44)[47] electrically coupled to the source, a drain contact terminal (46)[48] electrically coupled to the drain, and a well contact terminal (48)[49] electrically coupled to the second n- well.

Claim 46 relates to a p-channel floating-gate device, reciting a p- doped substrate (20),[50] a first n- well (22)[51] and a second n- well (24)[52] disposed in the substrate, a first p+ doped region (26)[53] disposed in the first n- well forming a source and a second p+ doped region (28)[54] disposed in the first n- well forming a drain, a channel (30)[55] disposed in the first n- well between source and drain, a third p+ doped region (36)[56] and a fourth (38)[57] p+ doped region disposed in the second n- well, the third p+ region and fourth p+ region together forming a tunneling junction. Claim 46 further recites a layer of gate oxide (32)[58] disposed above the channel, the first n- well and said second n- well, and a single polysilicon layer (16) disposed above the layer of gate oxide, the single polysilicon layer comprising a floating gate. Claim 46 further recites a source contact terminal (44) electrically coupled to the source, a drain contact terminal (46) electrically coupled to the drain, and a well contact terminal (48) electrically coupled to the second n- well.

Claim 47 relates to a system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system including a p-channel floating-gate device (11). The p-channel floating gate device comprises a p- doped substrate (20), a first n- well (22) and a second n- well (24) disposed in the substrate, a first p+ doped region (26) disposed in the first n- well forming a source and a second p+ doped region (28) disposed in the first n- well forming a drain, a channel (30) disposed in the first n- well between source and drain, a third p+

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[46] P. 11, ll. 2-6.
[47] P.11, l. 21.
[48] P. 11, l. 22.
[49] P. 11, l. 22.
[50] P. 10, ll. 18-19.
[51] P. 10, l. 19.
[52] P. 10, l. 20.
[53] P. 10, l. 21.
[54] P. 10, l. 21.
[55] P. 11, ll. 1-2.
[56] P. 11, l. 12.
[57] P. 11, l. 12.
[58] P. 11, l. 2.

doped region (36)[59] and a fourth (38)[60] p+ doped region disposed in the second n- well, the third p+ region and fourth p+ region together forming a tunneling junction. Claim 47 further recites a layer of gate oxide (32) disposed above the channel,[61] the first n- well and said second n- well, and a single polysilicon layer (16) disposed above the layer of gate oxide, the single polysilicon layer comprising a floating gate.[62] Claim 47 further recites a source contact terminal (44)[63] electrically coupled to the source, a drain contact terminal (46)[64] electrically coupled to the drain, and a well contact terminal (48)[65] electrically coupled to the second n- well.

Claim 48 relates to a p-channel floating gate device and recites a p- doped substrate (20),[66] a first n- well (22)[67] and a second n- well (24)[68] disposed in the substrate, a first p+ doped region (26)[69] disposed in the first n- well forming a source and a second p+ doped region (28)[70] disposed in the first n- well forming a drain, a channel (30)[71] disposed in the first n- well between source and drain, a third p+ doped region (36) and a fourth (38) p+ doped region disposed in the second n- well, the third p+ region and fourth p+ region together forming a tunneling junction. Claim 48 further recites a layer of gate oxide (32) disposed above the channel, the first n- well and the second n- well, a polysilicon floating gate (16) disposed above the layer of gate oxide, a source contact terminal (44) electrically coupled to the source, a drain contact terminal (46) electrically coupled to the drain, and a well contact terminal (48) electrically coupled to the second n- well.

Claim 50 relates to a p-channel floating gate device, and recites p- doped substrate (20), a first n- well (22) and a second n- well (24) disposed in the substrate, a first p+ doped region (26) disposed in the first n- well forming a source and a second p+ doped region (28) disposed in the

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[59] P. 11, l. 12.
[60] P. 11, l. 12.
[61] P. 11, l. 2.
[62] P. 11, ll. 2-6.
[63] P. 11, l. 22.
[64] P. 11, l. 22.
[65] P. 11, l. 22.
[66] P. 10, ll. 18-19.
[67] P. 10, l. 19.
[68] P. 10, l. 20.
[69] P. 10, l. 21.
[70] P. 10, l. 21.
[71] P. 11, ll. 1-2.

first n- well forming a drain, a channel (30)[72] disposed in the first n- well between source and drain, a third p+ doped region (36)[73] and a fourth (38)[74] p+ doped region disposed in the second n- well, the third p+ region and fourth p+ region together forming a tunneling junction. Claim 50 further recites a layer of gate oxide (32)[75] disposed above the channel, the first n- well and the second n- well, a polysilicon floating gate (16) disposed above the layer of gate oxide, [76] a source contact terminal (44) electrically coupled to the source, a drain contact terminal (46) electrically coupled to the drain, and a well contact terminal (48) electrically coupled to the second n- well.[77] The third p+ doped region and fourth p+ doped region are shorted together with a conductive layer (40)[78] which forms a bridge over the floating gate, the well contact terminal being strapped to the third p+ doped region and the fourth p+ doped region.

[72] P. 11, ll. 1-2.
[73] P. 11, l. 12.
[74] P. 11, l. 12.
[75] P. 11, l. 2.
[76] P. 11, ll. 2-6.
[77] P. 11, ll. 21-22.
[78] P. 11, l. 13.

Grounds of Rejection to be Reviewed on Appeal

Whether Claims 36-40 and 44-52 are unpatentable under 35 U.S.C. 103(a) over U.S. Pat. No. 6,563,731 (Bergemont) in view of U.S. Pat. No. 6,777,758 (Yamashita et al). (The Final Office Action initially identifies Claims 36-37, 39-49 and 51-52 as the rejected claims, but addresses Claims 36-40 and 44-52 in the body of the rejection. Applicants presume that the intent of the Final Office Action is to reject Claims 36-40 and 44-52 and that the initial identification of only Claims 36-40 and 44-52 is in error.)

Argument

According to M.P.E.P. § 2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Claims 36-37 and 44-48

The final Office Action fails to account for all the elements recited in the claims. For example, Claim 36 recites first (22) and second (24) n- wells. The final Office Action points to Bergemont's n- well 205 as the second n- well, and to the n- well to the left of that (presumably 203) as the first n- well. However, Claim 36 also recites first (26) and second p+ regions(28) in the first n- well *and third (36) and fourth (38) p+ regions in the second n- well*. Bergemont shows p+ regions in second n- well 205, but does NOT show any p+ regions in the n- well to the left of that (that is, n- well 203). Bergemont also does not show other claimed features *relating to the first n- well (22), which allegedly corresponds to n- well 203*, such as a channel (30) between a source (26) and a drain (28), a source contact terminal (44), and a drain contact terminal (46). While similar features are shown in relation to second n- well 205 of Bergemont,

none are show in relation to the first n- well (203) as Claim 36 and 44-48 expressly and clearly recite. Thus the interpretation that the Office Action seeks to take of Applicants' claims vis-à-vis Bergemont is fraught with inconsistencies and fails to account for all of features set forth in the claims. Only one of the missing features from Claims 36 and 44-48 is addressed in the Office Action—the well contact terminal (48) electrically coupled to the second n- well (24). The Office Action points to contact 32 of FIG. 1 of Yamashita as allegedly corresponding to this feature. However, the reasoning proffered for combining these references is unpursuasive. According to the Office Action, the combination of Bergemont and Yamashita is proper in order "to reduce the layout area of elements for fixing the potential of wells in a semiconductor device." But reducing layout area is always a desired goal in any semiconductor device, and its blanket assertion here to justify the combination of Bergemont and Yamashita ignores many factors that in fact make these references incompatible. Bergemont is directed to EEPROM memories. These operate on electron tunneling principals, primarily through gate oxides, and the conditions required to permit tunneling are very specific and impose strict limitations on operational, material and dimensional parameters. In addition, the object of Bergemont is realize a device that can be fabricated consistent with CMOS processing procedures (see for example col. 4, ll. 47-55; col. 2, ll. 40-44). Otherwise EEPROM devices can only be economically produced in bulk, and cannot be efficiently incorporated into SOC (system-on-chip) devices as Bergemont seeks to do. Yamashita, by comparison, is not concerned with CMOS processing and introduces numerous fabrication steps that are inconsistent with CMOS processing and would add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont. This argument was advanced previously by Applicants, but was mischaracterized in the final Office Action as advocacy of product-by-process claims. In fact there are no process steps recited in any of Applicant's claims and therefore none of them fall into the class of product-by-process claims. Applicant simply reasoned that the teachings of Bergemont and Yamashita are incompatible because they employ processes that are inconsistent with each other and with their stated goals of achieving products that are also different and incompatible. The object of Bergemont is to realize a device that can be fabricated consistent with CMOS processing procedures. Yamashita, by comparison, is not concerned with CMOS processing and introduces numerous fabrication steps that are inconsistent with CMOS processing and would add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont.

Accordingly, it is respectfully requested that the rejection of claims based on Bergemont and Yamashita be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Claim 38-40 and 50-52

The arguments above are equally applicable to Claims 38-40 and 50-52 because the obviousness rejection proposes to combine Bergemont and Yamashita to meet the limitations of these claims. However, as explained above, these references are not properly combinable. In addition, as in the argument above, the interpretation that the Office Action seeks to take of Applicants' claims vis-à-vis Bergemont is fraught with inconsistencies and fails to account for all of the features set forth in Claim 38 and 50. The exceptions in this case, which are allegedly remedied by Yamashita, are the third (36) and fourth (38) p+ doped regions which are shorted together with a conductive layer (40) which forms a bridge over the floating gate (16), and the well contact terminal (48) which is strapped to the third (36) and fourth (38) p+ doped regions.

Accordingly, it is respectfully requested that the rejection of claims based on Bergemont and Yamashita be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Claims Appendix

36. A pFET synapse transistor, comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said p- doped substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ doped region and said fourth p+ doped region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n- well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

37. A pFET synapse transistor in accordance with claim 36, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate.

38. A pFET synapse transistor, comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said p- doped substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ doped region and said fourth p+ doped region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n-well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate and wherein said well contact terminal is strapped to said third p+ doped region and said fourth p+ doped region.

39. A pFET synapse transistor in accordance with claim 38, wherein said transistor is formed with a single layer of conductive polysilicon.

40. A pFET synapse transistor in accordance with claim 36 fabricated using a standard CMOS process.

44. A pFET synapse transistor, comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n-well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well,

wherein said synapse transistor is configured to operate as a current source without gate input using a single polysilicon gate layer.

45. A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a pFET synapse transistor including:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n- well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

46. A p-channel floating-gate device, comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n- well;

a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon

layer comprising a floating gate;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

47. A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a p-channel floating-gate device, including:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n- well;

a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon layer comprising a floating gate;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

48. A p-channel floating gate device comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n-well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

49. (Previously presented) A p-channel floating gate device in accordance with claim 48, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate.

50. A p-channel floating gate device comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n-well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate wherein said well contact terminal is strapped to said third p+ doped region and said fourth p+ doped region.

51. A p-channel floating gate device in accordance with claim 50, wherein said transistor is formed with a single layer of conductive polysilicon.

52. A p-channel floating gate device in accordance with claim 48 fabricated using a standard CMOS process.

Evidence Appendix

None.

Related Proceedings Appendix

None.

Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-1698.

Respectfully submitted,

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